



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

09 994,293

11 26 2001

Abdalla Aly Naem

072219-0278251

9591

(P04976-P0)

33402

7590

07 09 2003

LAW OFFICES OF MARK C. PICKERING

P.O. BOX 300

PETALUMA, CA 94953

EXAMINER

FOONG, SUK SAN

ART UNIT

PAPER NUMBER

2823

DATE MAILED: 07 09 2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/994,293

Applicant(s)

NAEM, ABDALLA ALY

Examiner

Suk-San Foong

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☐ Claim(s) 1-15 and 19-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) 1, 5 and 6 is/are rejected.
- 7) ☐ Claim(s) 2-15 and 19-21 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on 8/16/02 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 6) ☐ Other: \_\_\_\_

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election without traverse of Group I, claims 1-15, in Paper No. 9 is acknowledged.

### *Drawings*

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "870" and "869" have both been used to designate sidewall spacers. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato ('280) in combination with Kameyama et al. ('227), Fitzgerald ('936) and Boyd et al. ('669).

Kato teaches a method of forming bipolar transistor which includes providing a collector layer of a first conductivity in an upper portion of silicon substrate 1 (Col. 5, lines 61-63, Col. 6

Art Unit: 2823

lines 29-31, and Fig. 4A), then forming trench 5 in the collector region (Col. 7, lines 1-17, and Fig. 4E), subsequently forming a layer of base material 7 comprised of silicon and germanium (Col. 7, lines 19-35, and Fig. 4F) and then removing portions of layer of base material 7 wherein a top surface of the layer of base material is coplanar with a top portion of the collector layer (Col. 7, lines 38-39 and Fig. 4G).

Kato does not teach forming a buried layer.

Kato does not teach forming an epitaxial layer having a smaller dopant concentration over the buried layer.

Kameyama et al. teaches a method of forming a bipolar transistor which includes providing semiconductor substrate 100 having buried layer 102 and epitaxial layer 104 wherein epitaxial layer has a smaller dopant concentration than buried layer 102 (Col. 6, lines 53-55, and Figs. 1 and 4A), then forming trench 142 (Col. 7, lines 12-16, and Fig. 4E), then forming a layer of base material 126 in trench 142 (Col. 7, lines 22-24, and Fig. 4E).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Kato with Kameyama et al. because it would enable forming a buried layer in the bipolar transistor device of Kato to be performed.

It would have been within the scope to one ordinary skill in the art to combine the teachings of Kato with Kameyama et al. because it would enable formation the collector layer of Kato to be performed.

The combination process does not teach chemically-mechanically polishing the base material.

Fitzgerald teaches a method of forming a semiconductor structure which includes providing silicon wafer 100 (Col. 3, lines 10-18, and Fig. 1A), then forming trench 102 in silicon wafer 100 (Col. 3, lines 27-30), then depositing a layer of base material 106, 108 comprised of silicon and germanium over silicon wafer 100 and trench 102 (Col. 3, lines 35-39, and Fig. 1B), and subsequently chemically-mechanically polishing wafer 100 so that base material 106, 108 is coplanar with surface of wafer 100 (Col. 3, lines 54-57, and Fig. 1C).

It would have been within the scope to one ordinary skill in the art to combine the teachings of the combination process with Fitzgerald because it would enable the step of removing portions of layer of base material 7 of Kato to be performed.

The combination process does not disclose forming a base protection material on the base material.

Boyd et al. teaches a method of forming integrated circuits which includes providing substrate 132 with trenches 140, 141 (Col. 4, lines 1-2, and Fig. 4), subsequently depositing second layer or layer of base material 160 of a semiconductor material over first layer 142 over substrate 132 thereby filling trenches 140, 141 (Col. 4, lines 7-10, and Fig. 5), subsequently forming layer of non-conductive base protection material 148, 150 on layer of base material 160 (Col. 3, lines 63-66, Col. 4, lines 12-15 and Fig. 5), subsequently chemically-mechanically polishing layer of base material 160 and layer of base protection material 148, 150 so that a top surface of layer of base protection material is coplanar with a top surface of substrate 132 (Col. 4, lines 19-23, and Fig. 5), and then selectively removing protection material 150 (Col. 4, lines 28-30, and Fig. 7).

It would have been within the scope to one ordinary skill in the art the combine the teachings of the combination process with Boyd et al. because it would the step of chemically-mechanically polishing silicon substrate 1 of the combination process to be performed and obtain further advantage of reducing and controlling the "dishing" associated with chemically-mechanically polishing process (Boyd et al., Col. 1, lines 62-65).

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kato ('280) in combination with Kameyama et al. ('227), Fitzgerald ('936) and Boyd et al. ('669) as applied to claims 1 and 5 above, and further in view of Chu et al. ('265).

The combination process does not teach the step recited in claim 6.

Chu et al. teaches forming bipolar transistors which includes forming a layer of base material 54 is comprised of silicon, germanium and carbon (Col. 4, lines 39-50, and Fig. 6).

It would have been within the scope to one ordinary skill in the art to combine the teachings of the combination process with Chu et al. because it would enable formation of the layer of base material 7 of the combination process to be performed and obtain further advantage of enhancing yield of SiGe and suppressing dislocations which cause bipolar pipe shorts (Chu et al., Col. 2, lines 45-47).

#### ***Allowable Subject Matter***

6. Claims 19 and claims dependent thereon are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Art Unit: 2823


***Conclusion***


7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suk-San Foong whose telephone number is 703-305-0383. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 (7724, 3431, 3432).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

  
June 25, 2003

  
George Fourson  
Primary Examiner  
Art Unit 2823